



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,661	05/14/2001	Masahiro Tanaka	208546US2	6508
22850	7590	04/30/2004	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			DIAZ, JOSE R	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/853,661	TANAKA, MASAHIRO	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-8 and 10-26 is/are pending in the application.
- 4a) Of the above claim(s) 6-8, 10-15 and 19-26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4,5 and 16-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>11/3/03</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed November 3, 2003 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Roman et al. (US Pat. No. 4,053,924).

Regarding claim 1, Roman et al. teaches an electrode contact section incorporated in a semiconductor device, comprising: a first-conductivity-type (N) semiconductor substrate (30) (see fig. 3); a second-conductivity-type impurity layer (P) formed in one surface of the semiconductor substrate (see fig. 2) and having a

Art Unit: 2815

thickness of not more than $1.0\text{ }\mu\text{m}$ (i.e. about $350\text{-}1000\text{ }\text{\AA}$)¹ from the one surface of the semiconductor substrate (see fig. 5); a second-conductivity-type (P+) contact layer (32) formed in the impurity layer (34) (see fig. 3) and having a thickness of not more than $0.2\text{ }\mu\text{m}$ (i.e. $300\text{-}800\text{ }\text{\AA}$) from the one surface of the semiconductor substrate (see fig. 5), the contact layer (32) being thinner than the impurity layer (34) (see fig. 3) and a peak of an impurity concentration of the contact layer (32) being higher than that of the impurity layer (34) (see fig. 5); a first electrode formed on the contact layer (36) (see fig. 3); and a second electrode (28) formed at another surface of the semiconductor substrate for allowing a current to flow between the first and second electrodes (see fig. 3).

Regarding claim 2, Roman et al. teaches the impurity layer is provided for carrier injection from the impurity layer to the semiconductor substrate, and the contact layer is provided for reducing a contact resistance between the first electrode and the impurity layer and not for carrier injection (see col. 3, lines 17-30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

¹ This range is the result of adding the thickness range of region 32 to the thickness range of region 34. For instance, region 32 has a maximum thickness value of $800\text{ }\text{\AA}$, and region 34 of $200\text{ }\text{\AA}$ (see fig. 5), thus, the total thickness for the region 34 is about $1000\text{ }\text{\AA}$.

Claims 1-2, 4-5, and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuwahara (US Pat. No. 5,44,271) in view of Roman et al. (US Pat. No. 4,053,924).

Regarding claims 1, 4, and 16, Kuwahara teaches an IGBT semiconductor device comprising: a first-conductivity-type semiconductor substrate (12) (see fig. 1); a second-conductivity-type base region (13-1, 13-2) formed in one surface of the semiconductor substrate (see fig. 1); a first-conductivity-type impurity region (14-1, 14-2, 14-3, 14-4) formed in the base region (see fig. 1); a first electrode (17-1, 17-2) connected to the first-conductivity-type impurity region (see fig. 1); a gate electrode (16-1) connected to the base region via an insulation film (15-1) (see fig. 1); a second-conductivity-type impurity region (11) formed in another surface of the semiconductor substrate (see fig. 1); a second-conductivity-type contact region (21) formed in the second-conductivity-type impurity region (see fig. 1) and having a thickness of not more than $0.2\text{ }\mu\text{m}$ from the another surface of the semiconductor substrate (see col. 6, lines 38-40), the contact region (21) being thinner than the second-conductivity-type impurity region (11) (see fig. 1) and a peak of an impurity concentration (i.e. $10^{18}\text{-}10^{20}\text{ cm}^{-3}$) of the second-conductivity-type contact region (21) being higher than that (i.e. $10^{16}\text{-}10^{18}\text{ cm}^{-3}$) of the second-conductivity-type impurity region (11) (see col. 6, lines 32-33 and 38-39); and a second electrode (19) formed on the contact region (see fig. 1).

However, Kuwahara fails to teach the limitation about the second-conductivity-type impurity region having a thickness of not more than $1.0\text{ }\mu\text{m}$ from another surface of the semiconductor substrate. Roman et al. teaches that it is very well known in the art to

reduce the thickness of a second-conductivity-type impurity region (34) to about not more than $1.0\text{ }\mu\text{m}$ (i.e. 350-1000 Å) (see fig. 5). Furthermore, Roman et al. teaches second-conductivity-type contact region (32) having a thickness of less than about $0.2\text{ }\mu\text{m}$ (i.e. 300-800 Å) (see fig. 5).

Kuwahara and Roman et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a second-conductivity-type impurity region having a thickness of more than $1.0\text{ }\mu\text{m}$. The motivation for doing so, as is taught by Roman et al., is to improve the forward and reverse recovery times of the junction without degrading the steady state reverse current characteristic (abstract). Therefore, it would have been obvious to combine Roman et al. with Kuwahara to obtain the invention of claims 1-2, 4-5, and 16-18.

Regarding claims 2 and 17, Kuwahara teaches the impurity layer is provided for carrier injection from the impurity layer to the semiconductor substrate, and the contact layer is provided for reducing a contact resistance between the first electrode and the impurity layer and not for carrier injection (see col. 7, lines 1-19).

Regarding claims 5 and 18, Kuwahara teaches that the second second-conductivity-type impurity region (11) is formed in the entire one surface of the semiconductor substrate (12) (see fig. 1).

Response to Arguments

Applicant's arguments with respect to claims 1-2, 4-5, and 16-18 have been considered but are moot in view of the new grounds of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Correspondence

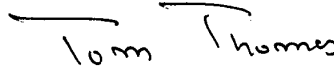
Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

Art Unit: 2815

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
4/21/04


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800